

1 1. (Currently Amended) An input buffer receiver comprising:

2 a buffer input portion for receiving an input signal, said buffer input

3 portion comprising a bias node;

4 a large capacitor between the bias node and a lower supply voltage

5 said large capacitor providing a coupling ratio between said

6 large capacitor and a parasitic capacitor coupled between said

7 bias node and a ground reference point approaching a unity

8 value such that a biasing voltage at said biasing node follows

9 said lower supply voltage to minimize effects of a ground noise

10 signal between the lower supply voltage and the ground

11 reference point; and

12 a buffer output portion in communication with the buffer input

13 portion for producing an output signal.

1 2. (Currently Amended) The input buffer receiver of claim 1, wherein the

2 buffer input portion which receives the input signal further comprises:

3 a first transistor of a first conductivity type having a source node to

4 which the lower supply voltage is applied, a gate node to which

5 a reference voltage is applied, and a drain node at which the

6 biasing voltage is developed ;

7 a second transistor of a second conductivity type having a drain
8 node which is connected to the drain node of the first transistor,
9 and a gate node at which the biasing voltage is developed, and
10 a source node to which an upper supply voltage source is
11 applied;

12 a third transistor of the second conductivity type having a drain
13 node which is connected to the drain of a fourth transistor, a
14 gate node at which the biasing voltage is developed, and a
15 source node to which the upper supply voltage source is
16 applied;

17 a fourth transistor of the first conductivity type having a source node
18 to which lower supply voltage is applied, a gate node to which
19 an input signal is applied externally, and a drain node which is
20 an input to the buffer output portion.

1 3. (Currently Amended) The input buffer receiver of claim 2, wherein the first
2 and fourth transistors are NMOS transistors, and the second and third
3 transistors are PMOS transistors.

1 4. (Currently Amended) The input buffer receiver of claim 2, wherein the
2 large capacitor is connected between the sources of the first and fourth
3 transistorsof the buffer input portion and the gate of the second transistor
4 of the buffer input portion.

- 1 5. (Currently Amended) The input buffer receiver of claim 2, wherein the gate
- 2 of the second transistor is connected to its drain.
- 1 6. (Currently Amended) The input buffer receiver of claim 2, wherein the gate
- 2 of the second transistor is connected to the drain of the first transistor.
- 1 7. (Currently Amended) The input buffer receiver of claim 2, wherein the gate
- 2 of the second transistor is connected to the gate of the third transistor.
- 1 8. (Currently Amended) The input buffer receiver of claim 2, wherein the
- 2 buffer output portion which produces output signal comprises: a first
- 3 inverter connected to the drain of the third transistor and the drain of the
- 4 fourth transistor;
- 1 9. (Currently Amended) The input buffer receiver of claim 2, wherein the third
- 2 transistor and the fourth transistor activate almost simultaneously to
- 3 minimize the effects of ground noise on a delay jitter factor of said input
- 4 buffer.
- 1 10. (Currently Amended) The input buffer receiver of claim 1, wherein the
- 2 large capacitor charge couples the bias node of the input buffer receiver to
- 3 the lower supply voltage of the input buffer receiver and wherein a
- 4 capacitance value of the large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 **CHC** is the capacitance value of the large capacitor,

8 and

9 **Cp** is the capacitance value of the parasitic capacitor.

1 11. (Currently Amended) The input buffer receiver of claim 1, wherein the
2 capacitance value of the large capacitor relative to said parasitic capacitor
3 results in a quicker response time for the output signal.

1 12. (New) An integrated circuit formed on a substrate comprising:
2 an input buffer receiver for receiving an input signal and connected
3 to said distribution network, said input buffer comprising:

4 a buffer input portion for receiving the input signal, said
5 buffer input portion comprising a bias node;
6 a large capacitor between the bias node and a lower
7 supply voltage, said large capacitor providing a
8 coupling ratio between said large capacitor and a
9 parasitic capacitor coupled between said bias node
10 and a ground reference point approaching a unity

11 value such that a biasing voltage at said biasing node
12 follows said lower supply voltage to minimize effects
13 of a ground noise signal between the lower supply
14 voltage and the ground reference point ; and

15 a buffer output portion in communication with the buffer
16 input portion for producing an output signal.

3 a first transistor of a first conductivity type having a source node to
4 which the lower supply voltage is applied, a gate node to which
5 a reference voltage is applied, and a drain node at which the
6 biasing voltage is developed :

7 a second transistor of a second conductivity type having a drain
8 node which is connected to the drain node of the first transistor,
9 and a gate node at which the biasing voltage is developed, and
10 a source node to which an upper supply voltage source is
11 applied;

12 a third transistor of the second conductivity type having a drain
13 node which is connected to the drain of a fourth transistor, a
14 gate node at which the biasing voltage is developed, and a

15 source node to which the upper supply voltage source is
16 applied;

17 a fourth transistor of the first conductivity type having a source node
18 to which lower supply voltage is applied, a gate node to which
19 an input signal is applied externally, and a drain node which is
20 an input to the buffer output portion.

1 14. (New) The integrated circuit of claim 13, wherein the first and fourth
2 transistors are NMOS transistors, and the second and third transistors are
3 PMOS transistors.

1 15. (New) The integrated circuit of claim 13, wherein the large capacitor is
2 connected between the sources of the first and fourth transistors of the
3 buffer input portion and the gate of the second transistor of the buffer input
4 portion.

1 16. (New) The integrated circuit of claim 13, wherein the gate of the second
2 transistor is connected to its drain.

1 17. (New) The integrated circuit of claim 13, wherein the gate of the second
2 transistor is connected to the drain of the first transistor.

1 18. (New) The integrated circuit of claim 13, wherein the gate of the second
2 transistor is connected to the gate of the third transistor.

- 1 19. (New) The integrated circuit of claim 13, wherein the buffer output portion
- 2 which produces output signal comprises: a first inverter connected to the
- 3 drain of the third transistor and the drain of the fourth transistor;
- 1 20. (New) The integrated circuit of claim 13, wherein the third transistor and
- 2 the fourth transistor activate almost simultaneously to minimize the effects
- 3 of ground noise on a delay jitter factor of said input buffer.
- 1 21. (New) The integrated circuit of claim 12, wherein the large capacitor
- 2 charge couples the bias node of the input buffer receiver to the lower
- 3 supply voltage of the input buffer receiver and wherein a capacitance
- 4 value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor,

8 and

9 Cp is the capacitance value of the parasitic capacitor.

- 1 22. (New) The integrated circuit of claim 12, wherein the capacitance value of
- 2 the large capacitor relative to said parasitic capacitor results in a quicker
- 3 response time for the output signal.

1 23. (New) A method for minimizing effects of ground noise on an input buffer
2 receiver comprising the steps of:

3 forming a buffer input portion for receiving an input signal on a
4 substrate;

5 forming a bias node within said buffer input portion;

6 connecting said a lower supply voltage to said buffer input portion;

7 forming a large capacitor between the bias node and the lower
8 supply voltage said large capacitor providing a coupling ratio
9 between said large capacitor and a parasitic capacitor coupled
10 between said bias node and a ground reference point
11 approaching a unity value such that a biasing voltage at said
12 biasing node follows said lower supply voltage to minimize
13 effects of a ground noise signal between the lower supply
14 voltage and the ground reference point; and

15 forming a buffer output portion on said substrate in communication
16 with the buffer input portion for producing an output signal.

1 24. (New) The method of claim 23, wherein forming the buffer input portion
2 further comprises the steps of:

3 forming a first transistor of a first conductivity type on said
4 substrate;
5 applying the lower supply voltage to a source node of the first
6 transistor;
7 applying a reference voltage to a gate node of the first transistor;
8 connecting a drain node of the first transistor to develop as biasing
9 voltage at said drain node;
10 forming a second transistor of a second conductivity type on said
11 substrate;
12 connecting a drain node of the second transistor to the drain node
13 of the first transistor;
14 connecting a gate node of the second transistor to the drain node of
15 the first transistor for developing the biasing voltage; and
16 connecting a source node of the second transistor to an upper
17 supply voltage;
18 forming a third transistor of the second conductivity type on said
19 substrate;

20 connecting a drain node of the third transistor to the drain of a
21 fourth transistor;

22 connecting a gate node of the third transistor to the drain node of
23 the first transistor for developing the biasing voltage;

24 connecting a source node of the third transistor to the upper supply
25 voltage source;

26 forming a fourth transistor of the first conductivity type on said
27 substrate;

28 connecting a source node of the fourth transistor to the lower
29 supply voltage;

30 connecting a gate node of the fourth transistor to receive an input
31 signal externally; and

32 connecting a drain node of the fourth transistor to an input to the
33 buffer output portion.

- 1 25. (New) The method of claim 24, wherein the first and fourth transistors are
2 NMOS transistors, and the second and third transistors are PMOS
3 transistors.

1 26. (New) The method of claim 24, wherein forming the large capacitor
2 comprises the step of:

3 connecting said large capacitor between the sources of the first and
4 fourth transistors of the buffer input portion and the gate of the
5 second transistor of the buffer input portion.

1 27. (New) The method of claim 24, wherein forming the buffer input portion
2 further comprises the steps of:

3 connecting the gate of the second transistor to its drain.

1 28. (New) The method of claim 24, wherein forming the buffer input portion
2 further comprises the steps of:

3 connecting the gate of the second transistor to the gate of the third
4 transistor.

1 29. (New) The method of claim 24, wherein forming the buffer output portion
2 which produces output signal comprises the step of:

3 forming a first inverter on said substrate; and

4 connecting an input of said first inverter to the drain of the third
5 transistor and the drain of the fourth transistor;

1 30. (New) The method of claim 24, wherein the third transistor and the fourth
2 transistor activate almost simultaneously to minimize the effects of ground
3 noise on a delay jitter factor of said input buffer.

1 31. (New) The method of claim 23, wherein the large capacitor charge
2 couples the bias node of the input buffer receiver to the lower supply
3 voltage of the input buffer receiver and wherein a capacitance value of the
4 large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor,
8 and

9 Cp is the capacitance value of the parasitic capacitor.

1 32. (New) The method of claim 23, wherein the capacitance value of the large
2 capacitor relative to said parasitic capacitor results in a quicker response
3 time for the output signal.

1 33. (New) An apparatus for minimizing effects of ground noise on an input
2 buffer receiver comprising:

3 means for forming a buffer input portion for receiving an input signal
4 on a substrate;

5 means for forming a bias node within said buffer input portion;

6 means for connecting said a lower supply voltage to said buffer
7 input portion;

8 means for forming a large capacitor between the bias node and the
9 lower supply voltage said large capacitor providing a coupling
10 ratio between said large capacitor and a parasitic capacitor
11 coupled between said bias node and a ground reference point
12 approaching a unity value such that a biasing voltage at said
13 biasing node follows said lower supply voltage to minimize
14 effects of a ground noise signal between the lower supply
15 voltage and the ground reference point; and

16 means for forming a buffer output portion on said substrate in
17 communication with the buffer input portion for producing an
18 output signal.

1 34. (New) The apparatus of claim 23, wherein forming the buffer input portion
2 further comprises:

3 means for forming a first transistor of a first conductivity type on
4 said substrate;

5 means for applying the lower supply voltage to a source node of the
6 first transistor;

7 means for applying a reference voltage to a gate node of the first
8 transistor;

9 means for connecting a drain node of the first transistor to develop
10 as biasing voltage at said drain node;

11 means for forming a second transistor of a second conductivity type
12 on said substrate;

13 means for connecting a drain node of the second transistor to the
14 drain node of the first transistor;

15 means for connecting a gate node of the second transistor to the
16 drain node of the first transistor for developing the biasing
17 voltage; and

18 means for connecting a source node of the second transistor to an
19 upper supply voltage;

20 means for forming a third transistor of the second conductivity type
21 on said substrate;

22 means for connecting a drain node of the third transistor to the
23 drain of a fourth transistor;

24 means for connecting a gate node of the third transistor to the drain
25 node of the first transistor for developing the biasing voltage;

26 means for connecting a source node of the third transistor to the
27 upper supply voltage source;

28 means for forming a fourth transistor of the first conductivity type on
29 said substrate;

30 means for connecting a source node of the fourth transistor to the
31 lower supply voltage;

32 means for connecting a gate node of the fourth transistor to receive
33 an input signal externally; and

34 connecting a drain node of the fourth transistor to an input to the
35 buffer output portion.

1 35. (New) The apparatus of claim 24, wherein the first and fourth transistors
2 are NMOS transistors, and the second and third transistors are PMOS
3 transistors.

1 36. (New) The apparatus of claim 24, wherein means for forming the large
2 capacitor comprises:

3 means for connecting said large capacitor between the sources of
4 the first and fourth transistors of the buffer input portion and the
5 gate of the second transistor of the buffer input portion.

1 37. (New) The apparatus of claim 24, wherein means for forming the buffer
2 input portion further comprises:

3 means for connecting the gate of the second transistor to its drain.

1 38. (New) The apparatus of claim 24, wherein means for forming the buffer
2 input portion further comprises the steps of:

3 means for connecting the gate of the second transistor to the gate
4 of the third transistor.

1 39. (New) The apparatus of claim 24, wherein means for forming the buffer
2 output portion which produces output signal comprises:

3 means for forming a first inverter on said substrate; and

4 means for connecting an input of said first inverter to the drain of
5 the third transistor and the drain of the fourth transistor;

1 40. (New) The apparatus of claim 24, wherein the third transistor and the
2 fourth transistor activate almost simultaneously to minimize the effects of
3 ground noise on a delay jitter factor of said input buffer.

1 41. (New) The apparatus of claim 23, wherein the large capacitor charge
2 couples the bias node of the input buffer receiver to the lower supply
3 voltage of the input buffer receiver and wherein a capacitance value of the
4 large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor
8 CHC, and

9 Cp is the capacitance value of the parasitic capacitor
10 Cp.

1 42. (New) The apparatus of claim 23, wherein the capacitance value of the
2 large capacitor relative to said parasitic capacitor results in a quicker
3 response time for the output signal.